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| EXAMINER | |
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| FINDLEY, CHRISTOPHER G | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/813,286 | COMPTON ET AL. | |
| | Examiner | Art Unit | |
| | CHRISTOPHER FINDLEY | 2621 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

***Response to Arguments***

1. Applicant's arguments filed 3/23/2009 have been fully considered but they are not persuasive.

2. Re claims 1-21 and 25-28, the Applicant contends that Zdepski is completely silent on the issue of phase synchronization. However, the Examiner respectfully disagrees. First, the Examiner directs the Applicant's attention to column 1, lines 50-54 of Zdepski, where it is disclosed that receivers typically include phase locked loops (PLLs). Additionally, Zdepski discloses that auxiliary packets are arranged to include differential count values based on a system modulo clock (Zdepski: column 2, lines 4-10), wherein "provision is made to measure the time, in counts of clock pulses of said system clock frequency, of the time the signal is delayed" (Zdepski: column 2, lines 10-16). The Merriam-Webster online dictionary defines phase as "the point or stage in a period of uniform circular motion, harmonic motion, or the periodic changes of any magnitude varying according to a simple harmonic law to which the rotation, oscillation, or variation has advanced from its standard position or assumed instant of starting" (http://www.merriam-webster.com/dictionary/phase, entry number 3). The Examiner asserts that the measurement of a time delay with reference to the original signal meets the definition of phase as stated above. Furthermore, the combination of the time delay offset value included in the auxiliary packet transmitted to the receiver (Zdepski: column 2, lines 4-16) with the phase locked loop disclosed by both Aweya (Aweya: column 1, lines 14-17)

and Zdepski (Zdepski: column 1, lines 50-54 and column 2, lines 19-27) render the disputed claims obvious.

3. Re claims 1-21 and 25-28, the Applicant contends that Zdepski does not describe the use of one timing packet to achieve phase synchronization. However, the Examiner respectfully disagrees. Zdepski discloses that auxiliary packets are arranged to include differential count values based on a system modulo clock (Zdepski: column 2, lines 4-10), thus indicating that that one such auxiliary packet indicates a difference in timing, measured with respect to the reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of a reference image synchronization signal, as claimed.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**5. Claims 10-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aweya et al. (US 7043651 B2) in view of Zdepski (US 5467137 A).**

Re **claim 1**, Aweya discloses a method of synchronizing the phase of a local image synchronization signal generator of a local video data processor in

communication with an asynchronous switched packet network to the phase of a reference image synchronization signal generator of a reference video data processor also coupled to said network, said local and reference processors having respective clocks, said reference and local image synchronization signal generators generating periodic image synchronization signals in synchronism with said reference and local clocks respectively, said method comprising the steps of: frequency synchronizing said local and reference clocks (Aweya: Abstract section); said reference video data processor sending, via said network, to said local data processor image timing packets providing reference image synchronization data indicating a difference in timing, measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of a reference image synchronization signal (Aweya: column 4, lines 57-62); and said local video data processor controlling the timing of production of said local image synchronization signals in dependence on said reference image synchronization data and a time of arrival of said image timing packets (Aweya: column 4, lines 62-67).

Aweya does not explicitly state that the timestamp transmitted by the transmitter includes a clock interval value. However, Zdepski discloses a method and apparatus for synchronizing a receiver as for a compressed video signal using differential time code, wherein Zdepski suggests that the transmitter embeds a differential count value indicative of a transmitter clock interval into an auxiliary timing packet for use by a receiver in order to synchronize the receiver clock (Zdepski: column 1, line 6, through column 2, line 27). Since both Aweya and Zdepski relate to calculating a difference

between a transmitter clock interval and a receiver clock interval for synchronization purposes, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the count value included in the auxiliary timing packet of Zdepski with the synchronization calculations disclosed by Aweya in order to lessen receiver processing load and improve efficiency by eliminating the need for the receiver to calculate the transmitter clock difference. The combined system of Awaya and Zdepski has all of the features of claim 1.

Re **claim 2**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 2, as discussed above in claim 1. Additionally, Aweya discloses that said controlling step comprises adjusting said time of production of said local image synchronization signal by a correction amount derived from a difference between said reference image synchronization data (Aweya: column 2, lines 54-60) and a time, measured with respect to said local processor's clock and said local image synchronization signal, of arrival of said timing packet (Aweya: column 2, lines 54-60).

Re **claim 3**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 3, as discussed above in claim 2. Additionally, Aweya discloses said reference processor sending to said local processor a plurality of said timing packets (Aweya: column 8, lines 22-32) from said reference processor; and controlling, by said local processor, said timing of said production of said local image synchronization signal in dependence on a function of said differences (Aweya: column 8, lines 22-45) between: reference image synchronization data in said timing packets;

and respective times of arrival of said timing packets at said local processor (Aweya: column 8, lines 22-45).

Re **claim 4**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 4, as discussed above in claim 3. Additionally, Aweya discloses that said function is an average of said differences (Aweya: column 8, lines 58-62).

Re **claim 5**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 5, as discussed above in claim 1. Additionally, Aweya discloses adding a delay to said local image synchronization signal (Aweya: column 5, lines 19-36).

Re **claim 6**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 6, as discussed above in claim 5. Additionally, Aweya discloses that said delay is a predetermined delay (Aweya: column 8, lines 22-45, the delay time is determined before clock synchronization occurs).

Re **claim 7**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 7, as discussed above in claim 1. Additionally, Aweya discloses sending to said local data processor from said reference processor, via said network, data packets containing said video data, said image timing packets being sent independently of said data packets (Aweya: column 3, lines 17-20).

Aweya does not explicitly state that said reference processor includes a source of video data produced synchronously with said reference processor's clock. However, Zdepski discloses a method and apparatus for synchronizing a receiver as for a

compressed video signal using differential time code, wherein Zdepski suggests that the transmitter embeds a differential count value indicative of a transmitter clock interval into an auxiliary timing packet for use by a receiver in order to synchronize the receiver clock (Zdepski: column 1, line 6, through column 2, line 27), wherein the data being transported is video data (Zdepski: column 3, lines 4-23). Since both Aweya and Zdepski relate to calculating a difference between a transmitter clock interval and a receiver clock interval for synchronization purposes, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the count value included in the auxiliary timing packet of Zdepski with the synchronization calculations disclosed by Aweya in order to lessen receiver processing load and improve efficiency by eliminating the need for the receiver to calculate the transmitter clock difference.

Re **claim 8**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 8, as discussed above in claim 1. Additionally, Aweya discloses sending to said local data processor from said reference processor, via said network, image timing packets containing said video data and also providing said reference image synchronization data (Aweya: column 3, lines 17-20). Aweya does not explicitly state that said reference processor includes a source of video data produced synchronously with said reference processor's clock. However, Zdepski discloses a method and apparatus for synchronizing a receiver as for a compressed video signal using differential time code, wherein Zdepski suggests that the transmitter embeds a differential count value indicative of a transmitter clock interval into an auxiliary timing packet for use by a receiver in order to synchronize the receiver clock (Zdepski: column

1, line 6, through column 2, line 27), wherein the data being transported is video data (Zdepski: column 3, lines 4-23). Since both Aweya and Zdepski relate to calculating a difference between a transmitter clock interval and a receiver clock interval for synchronization purposes, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the count value included in the auxiliary timing packet of Zdepski with the synchronization calculations disclosed by Aweya in order to lessen receiver processing load and improve efficiency by eliminating the need for the receiver to calculate the transmitter clock difference.

Re **claim 9**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 9, as discussed above in claim 1. Additionally, Aweya discloses sensing, by said reference processor, when said network has capacity to carry an image timing packet (Aweya: column 4, lines 21-29, queuing); and sending, from said reference processor, an image timing packet when such network capacity exists (Aweya: column 4, lines 21-29, queuing).

Re **claim 17**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 17, as discussed above in claim 1. Additionally, Aweya discloses aligning, in said local processor, an image of a video signal with said local image synchronization signal (Aweya: column 1, lines 51-53, the data may be video data).

Re **claim 19**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 19, as discussed above in claim 1. Additionally, Aweya discloses that said reference image synchronization data indicates a difference in timing,

measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of an immediately preceding reference image synchronization signal (Aweya: column 8, lines 22-45, times n and n-1 are used for calculation).

Re **claim 20**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 20, as discussed above in claim 1. Additionally, Aweya discloses that timing packets carrying information relating to at least two image synchronization signals are launched onto said network (Aweya: column 4, lines 57-67, the synchronization of the local clock is calculated from the difference between two time stamps sent by the transmitter).

Re **claim 21**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 21, as discussed above in claim 1. Additionally, Aweya discloses computer software comprising program code for carrying out a method according to claim 1 (Aweya: column 5, lines 38-41).

Re **claim 25**, Aweya discloses a video network comprising: a reference video data processor including a reference image synchronization signal generator and a reference clock generator, said reference synchronization signal generator configured to generate periodic image synchronization signals in synchronism with said reference clock (Aweya: column 4, lines 57-62); a local video data processor including a local image synchronization signal generator and a local clock generator frequency-locked to said reference clock generator, said local synchronization signal generator configured to

generate periodic image synchronization signals in synchronism with said local clock (Aweya: column 4, lines 62-67); an asynchronous packet-based network linking said local processor and said reference processor (Aweya: column 3, lines 9-13); said reference video data processor includes a sending unit configured to send, via said network, to said local data processor an image timing packet providing reference image synchronization data indicating a difference in timing, measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time of production of a reference image synchronization signal (Aweya: column 3, lines 39-42); and said local processor including a controlling unit configured to adjust the phase of production of said local image synchronization signal in dependence on said reference image synchronization data and said time of arrival of said timing packet (Aweya: column 8, lines 22-45).

Aweya does not explicitly state that the timestamp transmitted by the transmitter includes a clock interval value embedded in one image timing packet. However, Zdepski discloses a method and apparatus for synchronizing a receiver as for a compressed video signal using differential time code, wherein Zdepski suggests that the transmitter embeds a differential count value indicative of a transmitter clock interval into an auxiliary timing packet for use by a receiver in order to synchronize the receiver clock (Zdepski: column 1, line 6, through column 2, line 27). Since both Aweya and Zdepski relate to calculating a difference between a transmitter clock interval and a receiver clock interval for synchronization purposes, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the count value included in

the auxiliary timing packet of Zdepski with the synchronization calculations disclosed by Aweya in order to lessen receiver processing load and improve efficiency by eliminating the need for the receiver to calculate the transmitter clock difference.

Re **claim 26**, Aweya discloses a local video data processor including a local image synchronization signal generator and a local clock generator frequency-lockable to a reference clock generator at a reference video data processor and configured to connect to said local video data processor via an asynchronous packet-based network, said local synchronization signal generator configured to generate periodic image synchronization signals in synchronism with said local clock (Aweya: column 8, lines 1-45), said local video data processor comprising: a controlling unit configured to adjust the phase of production of said local image synchronization signal in dependence on a received timing packet providing reference image synchronization data received provided by the image timing packet from said reference clock generator and a time of arrival of the image timing packet (Aweya: column 4, lines 57-67).

Aweya does not explicitly state that the timestamp transmitted by the transmitter includes a clock interval value embedded in one image timing packet. However, Zdepski discloses a method and apparatus for synchronizing a receiver as for a compressed video signal using differential time code, wherein Zdepski suggests that the transmitter embeds a differential count value indicative of a transmitter clock interval into an auxiliary timing packet for use by a receiver in order to synchronize the receiver clock (Zdepski: column 1, line 6, through column 2, line 27). Since both Aweya and Zdepski relate to calculating a difference between a transmitter clock interval and a

receiver clock interval for synchronization purposes, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the count value included in the auxiliary timing packet of Zdepski with the synchronization calculations disclosed by Aweya in order to lessen receiver processing load and improve efficiency by eliminating the need for the receiver to calculate the transmitter clock difference.

Re **claim 27**, Aweya discloses a reference video data processor, comprising: a reference image synchronization signal generator and a reference clock generator; said reference synchronization signal generator configured to generate periodic image synchronization signals in synchronism with said reference clock; said reference processor configured to connect via an asynchronous packet-based network to a local video data processor having a local image synchronization signal generator and a local clock generator frequency-lockable to said reference clock generator, said local synchronization signal generator configured to generate periodic image synchronization signals in synchronism with said local clock (Aweya: column 8, lines 1-45).

Aweya does not explicitly state that said reference video data processor including a phase synchronization unit configured to synchronize a phase of the local image synchronization signal generator and a phase of the reference synchronization generator by sending, via said network, to said local data processor one image timing packet providing reference image synchronization data indicating a difference in timing, measured with respect to said reference processor's clock, between a time at which said one image timing packet is launched onto said network and a time of production of a reference image synchronization signal. However, Zdepski discloses a method and

apparatus for synchronizing a receiver as for a compressed video signal using differential time code, wherein Zdepski suggests that the transmitter embeds a differential count value indicative of a transmitter clock interval into an auxiliary timing packet for use by a receiver in order to synchronize the receiver clock (Zdepski: column 1, line 6, through column 2, line 27). Since both Aweya and Zdepski relate to calculating a difference between a transmitter clock interval and a receiver clock interval for synchronization purposes, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the count value included in the auxiliary timing packet of Zdepski with the synchronization calculations disclosed by Aweya in order to lessen receiver processing load and improve efficiency by eliminating the need for the receiver to calculate the transmitter clock difference.

Re **claim 28**, the combined system of Aweya and Zdepski discloses an asynchronous switched network comprising a plurality of nodes, at least one of which nodes is coupled a reference data processor and at least one other of which is coupled to a local data processor (Aweya: Figs. 1 and 2A).

Re **claim 29**, Aweya discloses a computer readable medium encoded with a reference timing packet for use in an asynchronous switched packet network in which packets of video data are transmitted from a source to a destination, said packet providing a destination address of a processor and reference image synchronization data, measured with respect to a reference clock, between a time at which said packet is launched onto said network and a time of production a reference image synchronization signal (Aweya: column 3, lines 17-20; column 4, lines 57-67).

Aweya does not explicitly state that the timestamp transmitted by the transmitter includes a clock interval value. However, Zdepski discloses a method and apparatus for synchronizing a receiver as for a compressed video signal using differential time code, wherein Zdepski suggests that the transmitter embeds a differential count value indicative of a transmitter clock interval into an auxiliary timing packet for use by a receiver in order to synchronize the receiver clock (Zdepski: column 1, line 6, through column 2, line 27). Since both Aweya and Zdepski relate to calculating a difference between a transmitter clock interval and a receiver clock interval for synchronization purposes, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the count value included in the auxiliary timing packet of Zdepski with the synchronization calculations disclosed by Aweya in order to lessen receiver processing load and improve efficiency by eliminating the need for the receiver to calculate the transmitter clock difference.

**6. Claims 10-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aweya et al. (US 7043651 B2) in view of Zdepski (US 5467137 A) as applied to claims 10-16 and 18, and further in view of Lahat (US 6963561 B1).**

Re **claim 10**, the combined system of Awaya and Zdepski discloses a majority of the features of claim 10, as discussed above in claim 1. Additionally, Aweya discloses a that said step of frequency synchronizing said local and reference clocks includes the steps of: sending to said local data processor from said reference processor, via said

network, clock timing packets of said local processor and reference clock data indicating a time at which said clock timing packet is sent (Aweya: column 8, lines 22-32); and controlling, by said local processor, said frequency of said local processor's clock in dependence on said reference clock data and times of arrival of said clock timing packets (Aweya: column 8, lines 33-45).

Aweya does not specifically disclose that each packet provides a destination address. However, Lahat discloses a facility for transporting TDM streams over an asynchronous Ethernet network using internet protocol, wherein the UDP header, the TCP header, and the IP header all contain destination information (Lahat: Figs. 13, 14, and 15). Since Aweya, Zdepski, and Lahat relate to transmitting TDM packets over asynchronous networks, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the header addressing of Lahat with the combined synchronization system of Aweya and Zdepski in order to provide IP based voice and data transmission over a legacy network, thereby allowing for more efficient utilization of the network, and in turn providing the capability for new services for customers (Lahat: column 4, lines 57-65). The combined system of Aweya, Zdepski, and Lahat has all of the features of claim 10.

Re **claim 11**, the combined system of Aweya, Zdepski, and Lahat discloses a majority of the features of claim 11, as discussed above in claim 10, and additionally Aweya discloses counting cycles of said reference processor's clock (Aweya: column 3, lines 40-42), by said reference processor; and setting, by said reference processor, said reference clock data as said count of cycles of said reference processor's clock in

dependence on a time at which said clock timing packet containing said reference clock data is launched onto said network (Aweya: column 3, lines 40-42, transmitter clock used to generate timestamps).

Re **claim 12**, the combined system of Aweya, Zdepski, and Lahat discloses a majority of the features of claim 12, as discussed above in claim 11, and additionally Aweya discloses counting cycles of said local processor's clock (Aweya: column 5, lines 58-63), by said local processor; generating, by said local processor, local clock data as a count of cycles of said local processor's clock at a time of receipt of a clock timing packet containing reference clock data (Aweya: column 5, lines 58-63); and controlling, by said local processor, said local processor's clock in dependence on an error signal dependent on a difference between said reference clock data in successively received timing packets and a difference between local clock data indicating said local clock time at said times of receipt of said timing packets (Aweya: column 8, lines 33-45).

Re **claim 13**, the combined system of Aweya, Zdepski, and Lahat discloses a majority of the features of claim 13, as discussed above in claim 12, and additionally Aweya discloses low pass filtering said error signal to generate a low-pass filtered error signal (Aweya: column 8, lines 58-62).

Re **claim 14**, the combined system of Aweya, Zdepski, and Lahat discloses a majority of the features of claim 14, as discussed above in claim 13, and additionally Aweya discloses receiving said low-pass filtered error signal (Aweya: column 8, lines 58-62, an average requires accumulation of data) in said local processor; and

controlling, by said local processor, said local processor's clock in dependence on said received error signal (Aweya: column 8, lines 42-45).

Re **claim 15**, the combined system of Aweya, Zdepski, and Lahat discloses a majority of the features of claim 15, as discussed above in claim 10. Aweya does not specifically disclose that said clock timing packet containing said reference image synchronization data is independent of said reference clock data. However, Zdepski discloses a method and apparatus for synchronizing a receiver as for a compressed video signal using differential time code, wherein Zdepski suggests that the transmitter embeds a differential count value indicative of a transmitter clock interval into an auxiliary timing packet for use by a receiver in order to synchronize the receiver clock (Zdepski: column 1, line 6, through column 2, line 27), wherein the data being transported is video data containing an independent presentation time stamp (Zdepski: column 3, lines 4-23). Since both Aweya and Zdepski relate to calculating a difference between a transmitter clock interval and a receiver clock interval for synchronization purposes, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the count value included in the auxiliary timing packet of Zdepski with the synchronization calculations disclosed by Aweya in order to lessen receiver processing load and improve efficiency by eliminating the need for the receiver to calculate the transmitter clock difference.

Re **claim 16**, the combined system of Aweya, Zdepski, and Lahat discloses a majority of the features of claim 16, as discussed above in claim 10, and additionally Aweya discloses that said timing packet containing said reference image

synchronization data also contains said reference clock data (Aweya: column 3, lines 17-20).

Re **claim 18**, the combined system of Aweya and Zdepski discloses a majority of the features of claim 18, as discussed above in claim 1. Aweya does not specifically disclose that said image synchronization signal is a field or frame synchronization signal. However, Lahat discloses a facility for transporting TDM streams over an asynchronous Ethernet network using internet protocol, wherein packet arrival jitter is measured on a per frame basis (Lahat: column 18, lines 27-31). Since both Aweya and Lahat relate to transmitting TDM packets over asynchronous networks, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the header addressing of Lahat with the synchronization system of Aweya in order to provide IP based voice and data transmission over a legacy network, thereby allowing for more efficient utilization of the network, and in turn providing the capability for new services for customers (Lahat: column 4, lines 57-65). The combined system of Aweya and Lahat has all of the features of claim 18.

***Contact***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER FINDLEY whose telephone number is (571)270-1199. The examiner can normally be reached on Monday-Friday (8:30 AM-5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on 571-272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Marsha D. Banks-Harold/
Supervisory Patent Examiner, Art Unit 2621

/Christopher Findley/